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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,906	08/12/2004	Jen-Chieh Kao	11184-US-PA	4905
31561	7590	09/26/2006	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			DAVIS, ROBERT B	
			ART UNIT	PAPER NUMBER
			1722	
DATE MAILED: 09/26/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/710,906

Applicant(s)

KAO ET AL.

Examiner

Robert B. Davis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 6 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by James et al (6,969,918: figures 2A-7B; column 5, lines 4-56; column 6, lines 1-27; and column 7, lines 31-50).

James et al teach a mold for encapsulating semiconductor devices (56) mounted on a packaging substrate (46), the mold comprising: a top mold (42U) having a top runner (96U) and a plurality of mold cavities (86U) that are connected to the top runner and located correspondingly to the semiconductor devices; and a bottom mold (42L) having a lower dummy runner (110L). The upper mold also has an upper dummy runner (110U), an upper dummy cavity (102U) and a connecting dummy runner (100U). The lower mold has a connecting cavity dummy runner (114L), a lower dummy mold cavity (102L) and a lower dummy runner (110L). The mold has three different dummy cavities; connecting dummy segment (78), second lower dummy segment (118), and upper dummy segment (80). The upper mold cavity plate (42U) and the lower mold cavity plate (42L) are separated by the leadframe (46) as illustrated by Figure 2C and

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the product with upper and lower molded resin as illustrated by Figure 7B. The mold cavities (86U) are identical and located in a 1x2 array.

3. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by James et al.

James et al teach a packaging substrate (leadframe 46) for supporting a plurality of semiconductor dice (56), wherein the packaging substrate has a plurality of openings. Opening (64) corresponds to the top runner. Opening (70) corresponds to the dummy runner (78) and opening (72) corresponds to the dummy cavities (102U and 102L).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (JP 02-143816 A: figures 1-2 and the two English abstracts) taken together with James et al.

Takahashi discloses a process of forming a plurality of moisture-resistant molded articles comprising: providing a molding apparatus having an array of molding cavities (18) connected to a pot (12) by runners (15, 17) and dummy runners (20) that extend vertically between the runners (17) and horizontally between a portion adjacent the pot (12) to a vent (21). The reference states that the presence of the dummy runners improves moisture resistance by limiting voids in the molded article. The abstracts of the reference do not disclose the use of a leadframe and a semiconductor element, but it is clear that the cavity array, the pot and the problems of voids and moisture resistance are commonly known in the semiconductor encapsulation or packaging art. The reference teaches injecting molding compound (13) into a plurality of cavities (18) through runners (15, 17)

James et al teach a process of providing a packaging substrate (46) having a first surface (47U) and a second surface (47L), wherein the first surface (47U) has a semiconductor dice (56) disposed thereon; placing the packaging substrate inside a mold (40) so that a plurality of molding compounds (74) are formed on the first surface of the substrate (46), wherein dummy structures are formed on the top and bottom surface of the leadframe simultaneously.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the process of Takahashi by supplying a leadframe with a plurality of

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semiconductor elements into a mold such that the leadframe splits the upper and lower molding cavities in half as disclosed by James et al for the purpose of forming an array of elements having encapsulating resin on the upper and lower surfaces of the leadframe.

7. Claims 2-4, 7, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al taken together with Takahashi.

James et al disclose all claimed features except for the dummy runner connected to the top runner and the dummy runner extends into a space between the mold cavities, wherein the dummy runner extends in a direction perpendicular to the top runner, or a pot located within the top and bottom mold.

Takahashi discloses a mold having a pot (12), a plurality of mold cavities (18) connected by runners (15, 17) to the pot and a dummy runner (20) that extends both perpendicular and parallel to the runner (17).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of James et al by using a pot, runner and dummy runner in a mold as disclosed by Takahashi for the purpose of providing resin to a plurality of molding cavities simultaneously while avoiding voids by using the dummy runners.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi taken together with James et al as applied to claims 14 and 18 above, and further in view of Shikagawa et al (5,401,155: figures 1 and 3 and column 1, lines 13-27).

The combination of Takahashi and James et al disclose all claimed features except for the use of a transparent molding resin.

Shikagawa et al disclose a method of encapsulating a semiconductor laser element (1) with a transparent casting resin for the purpose of transmitting light through the resin package.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the process of the previous combination by using a transparent casting resin to form an optical packaged element for the purpose of allowing the product to transmit light to/from the element through the resin.

9. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi taken together with James et al as applied to claims 14 and 18 above, and further in view of Masuda et al (4,862,246: figures 1C, 2B, 2C and column 2, line 63 to column 3, line 39).

The combination of Takahashi and James et al disclose all claimed features except for the formation of grooves in the front and back surfaces of the leadframe to increase adhesion.

Masuda et al disclose a method of encapsulating a semiconductor chip on a leadframe (10) having depressions (11) formed on the back and front surfaces of the leadframe for the purpose of improving adhesion between the leadframe and the sealer resin.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the process of the previous combination by forming depressions or

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grooves in the front and back surfaces of the leadframe as disclosed by Masuda et al for the purpose of improving the adhesion between the sealing resin and the leadframe.

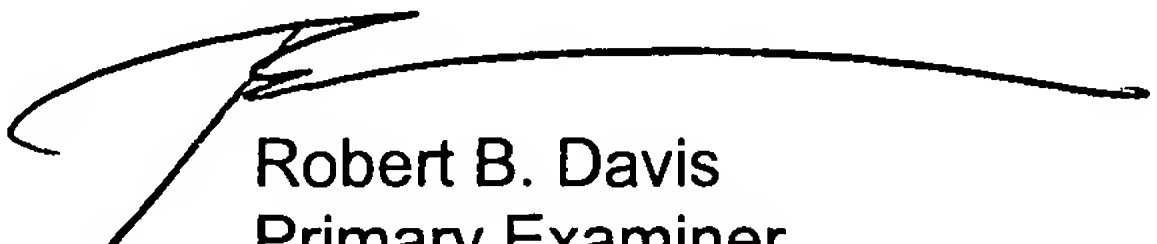
Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Davis whose telephone number is 571-272-1129. The examiner can normally be reached on Monday-Friday 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Robert B. Davis
Primary Examiner
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9/22/06